Remarks

Applicant respectfully requests reconsideration of this application as amended. Claims 1, 10, and 21 have been amended. No claims have been cancelled or added. Claims 6, 17, and 28 were previously canceled. Therefore, claims 1-5, 7-16, 18-27, and 29-33 are presented for examination.

35 U.S.C. §102(e) Rejection

Claims 1-5, 7-16, 18-27 and 29-33 stand rejected under 35 U.S.C. §102(b) as being anticipated by Sih et al. (U.S. Patent No. 6,606,700). Applicant submits that the present claims are patentable over Sih.

Sih discloses a digital signal processor architecture that is designed to speed up frequently-used signal processing computations, such as FIR filters, correlations, FFTs, and DFTs. The architecture uses a coupled dual-MAC architecture and attaches a dual-MAC coprocessor onto it in such a way as to achieve an increase in processor capability. (Sih at col. 1, ll. 49-55.)

Claim 1 recites:

> A method comprising:
> receiving input data by a processor;
> performing one or more current multiply-accumulate operations on the received input data with one or more modular multiply-accumulate units that are dynamically reconfigurable based, at least in part, on bandwidth requirements of the one ore more multiply accumulate operations; and
> saving the received input data for one or more multiply-accumulate operations to be performed after the current multiply-accumulate operations.

Applicant submits that Sih does not disclose or suggest performing one or more current multiply-accumulate operations on the received input data with one or more modular

multiply-accumulate units that are dynamically reconfigurable based, at least in part, on bandwidth requirements of the one ore more multiply accumulate operations, as recited by claim 1. Applicant can find no disclosure or suggestion of such a feature anywhere in Sih. Specifically, Shi does not provide for implementing multiply-accumulate units in a dynamic and modular manner based on bandwidth needs. Therefore, Sih does not disclose or suggest the above-cited feature of claim 1. As a result, claim 1, as well as its dependent claims, is patentable over Sih.

Independent claims 10 and 21 also recite, in part, performing one or more current multiply-accumulate operations on the received input data with one or more modular multiply-accumulate units that are dynamically reconfigurable based, at least in part, on bandwidth requirements of the one ore more multiply accumulate operations. As discussed above, Sih does not disclose or suggest such features. Therefore, claims 10 and 21, as well as their respective dependent claims, are patentable over Sih for the reasons discussed above with respect to claim 1.

Applicant respectfully submits that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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